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EXAMINER	
FRANKLIN, RICHARD B	
ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/643,622	FENG, EUGENE	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 9 are pending.

Response to Arguments

2. Applicant's arguments filed 01 March 2007 have been fully considered but they are not persuasive.

With regards to claims 1, 2, 7, and 9, Applicant has argued that the relied upon reference, US Patent No. 6,851,014 (hereinafter Chang), does not teach a controller circuit for controlling the memory cells and that is configured in response to the plurality of protocol signals. Applicant states that a "host controller" actually controls the operation of the memory cells (See Arguments; Page 7 Paragraph 2). However, the Examiner respectfully disagrees. Chang teaches that a host controller uses either one protocol or another, but does not teach that the host controller controls the memory array. Rather, Chang teaches that either the LPC Protocol Circuit (Chang; Figure 2 Item 208) or the FWH Protocol Circuit (Chang; Figure 2 Item 206) control the operation of the memory cells (Chang; Col 7 Lines 43 – 46 and 56 – 58). The Protocol Circuits are selected by the Protocol Detection Circuit (Figure 2 Item 201) to communicate with the memory array depending on which protocol the host controller is operating in (Chang; Col 8 Lines 41 – 48).

As per Applicant's arguments to the rejection of claims 3 – 6, and 8 under 35 USC 103(a), the Examiner has clearly shown that the elements of claims 1, 2, 7, and 9 are taught by Chang, and therefore, the rejection is believed to be proper.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 2, 7, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,851,014 (hereinafter Chang).

As per claim 1, Chang teaches a memory device (Figure 9 Item 900) for interfacing with an integrated circuit communicating via a communication bus (Figure 9 Items 203 and 205), the device comprising a decoding circuit (Figure 9 "Protocol Detection CKT") for receiving communication signals received via the communication bus, for decoding the communication signals and for generating a plurality of protocol signals (Figure 9 "SEL," Col 2 Line 65 – Col 3 Line 1) in response thereto; a protocol select circuit for receiving the plurality of signals (Figure 9 Item 902); an array of memory cells (Figure 9 Item 202); a controller circuit for controlling the operation of the array of memory cells (Figure 9 Items 206 and 208, Col 7 Lines 43 – 46, and Col 7 Lines 56 – 58); the protocol select circuit for configuring the controller circuit in response to the plurality of protocol signals (Col 7 Lines 43 – 46, Col 7 Lines 56 – 58, and Col 8 Lines 41 – 48).

As per claim 2, Chang also teaches wherein the memory cells are non-volatile memory cells (Col 4 Lines 30 – 34).

As per claim 7, Chang teaches a memory device (Figure 9 Item 900) for interfacing with an integrated circuit communicating via an LPC bus, the circuit generating a start field (Col 5 Lines 54 – 59), the device comprising a decoding circuit (Figure 9 "Protocol Detection CKT") for receiving the start field and for generating a plurality of protocol signals (Figure 9 "SEL," Col 2 Line 65 – Col 3 Line 1); a protocol select circuit for receiving the plurality of protocol signals (Figure 9 Item 902); an array of non-volatile memory cells (Figure 9 Item202, Col 4 Lines 30 – 34); a controller circuit for controlling the operation of the array of non-volatile memory cells (Figure 9 Items 206 and 208, Col 7 Lines 43 – 46, Col 7 Lines 56 – 58); the protocol select circuit for configuring the controller circuit in response to the plurality of protocol signals (Col 7 Lines 43 – 46, Col 7 Lines 56 – 58, and Col 8 Lines 41 – 48).

As per claim 9, Chang also teaches wherein the plurality of protocol signals represent protocol for LPC communication and for FWH communication (Col 5 Lines 44 – 48).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 5, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,851,014 (hereinafter Chang) in view of US Patent No. 4,789,984 (hereinafter Swartz). "Micro-Electronics – Digital and Analog Circuits and Systems" by Jacob Millman (hereinafter Millman).

As per claim 3, Chang teaches the memory device as described per claim 2 (See rejection of claim 2 above). Chang also teaches wherein the protocol select circuit is a multiplexer.

Chang does not teach wherein the protocol select circuit is a volatile storage element.

However, Swartz teaches a multiplexer that includes input latches (Figure 4 Items 4A1 and 4A2) and an output buffer (Swartz; Figure 4 Item 404, Col 5 Lines 59 – 64). Both input latches and output buffer are volatile storage elements.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Chang to include the volatile storage element because doing so allows the circuit to simultaneously sample or acquire new input data from the inputs (Swartz; Col 6 Lines 5 – 7).

As per claim 5, Swartz also teaches wherein the latches are flip-flops (Swartz; Col 5 Lines 14 – 19).

As per claim 8, Chang teaches the memory device as described per claim 7 (See rejection of claim 7 above). Chang also teaches wherein the protocol select circuit is a multiplexer.

Chang does not teach wherein the protocol select circuit is a volatile storage element.

However, Swartz teaches a multiplexer that includes input latches (Figure 4 Items 4A1 and 4A2) and an output buffer (Swartz; Figure 4 Item 404, Col 5 Lines 59 – 64). Swartz also teaches wherein the latches are flip-flops (Swartz; Col 5 Lines 14 – 19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Chang to include the flip-flops because doing so allows the circuit to simultaneously sample or acquire new input data from the inputs (Swartz; Col 6 Lines 5 – 7).

5. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,851,014 (hereinafter Chang) in view of US Patent No. 4,789,984 (hereinafter Swartz) and further in view of "Micro-Electronics – Digital and Analog Circuits and Systems" by Jacob Millman (hereinafter Millman).

As per claim 4, Chang in combination with Swartz teaches the memory device as described per claim 3 (See rejection of claim 3 above).

Chang in combination with Swartz does not teach wherein the volatile storage element is a register.

However, Millman teaches wherein a volatile storage element is a register (Millman; Pages 215 – 220 Section 7-4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Chang in combination with Swartz to include the register because doing so allows for the storage of more than one bit at a time (Millman; Page 215 Paragraph 1).

As per claim 6, Chang in combination with Swartz teaches the memory device as described per claim 3 (See rejection of claim 3 above).

Chang in combination with Swartz does not teach wherein the volatile storage element is an SRAM.

However, Millman teaches wherein a volatile storage element is a Static RAM (SRAM) (Millman; Pages 291 – 293 Section "Static MOS RAM").

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Chang in combination with Swartz to include the SRAM because doing so allows for the storage of kilobits of data at a time (Millman; Page 293 Paragraph 3).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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